The Nucleus **50**, No. 4 (2013) 341-350

The Nucleus
A Quarterly Scientific Journal of Pakistan Atomic Energy Commission
NCLEAM, ISSN 0029-5698

ACCURATE POWER ANALYSIS FOR CONVENTIONAL MOS TRANSISTORS USING 0.12µm TECHNOLOGY

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(Received July 04, 2013 and accepted in revised form November 19, 2013)

Power dissipation of very large scale integrated circuits (VLSI) has emerged as a significant constraint on the semiconductor industry. For the dynamic power the voltage, capacitance and frequency are the major components of the power dissipation. In this paper, we propose a new power macromodeling technique for the power estimation of conventional metal-oxide- semiconductor (MOS) transistors. As the dynamic power is directly linked with the load capacitance (C_L), it is also a lumped capacitance of all internal parasitic capacitances. In our proposed model, we take an account of the parasitic capacitances with their dependence on channel width and the length. Suitable values of other factors (i.e. threshold voltage V_T, gate voltage V_{GS}, drain voltage V_{DD} etc.) are used for the power consumption of the MOS transistors. The Preliminary results are effective and our macromodel provides the accurate power estimation.

Keywords *:* MOS transistor, Power estimation, Parasitic capacitances, Power dissipation, Macromodel

1. Introduction

Over the years, a considerable research and development efforts have been dedicated to modelling MOS devices in an accurate way. One of the key objectives of the modelling is to evaluate the current I_{ds} which flows between the drain and the source, depending on the supply voltages. A second objective of MOS model is to estimate the value of parasitic capacitances as shown in Figure 1. These capacitances vary with the voltages. The variation of the capacitances must be computed at each iteration of the analog simulations, to facilitate the prediction of switching delay.

In response to second objective, the parasitic capacitances are becoming an important issue for designing the logic circuits with aggressive reduction of MOS transistor dimensions into the deep sub micrometer regime [1-4]. In digital applications, these parasitic capacitances have strong impact on propagation delay and overall power dissipation of the circuit. For an analog application these capacitances causes a negative feedback which again have an influence on gain-bandwidth product. Due to their important role in short channel region, the parasitic capacitances are required to compute accurately to predict the circuit performance.

Several models for parasitic capacitances have been proposed. With precise mathematical iterations, Kamchouchi et al. [5] derived semi-empirical model by using Schwartz-Christoffel transformation. Considering conformal transformation Shrivastava et al. [6] developed a simple analytical model with the assumption that the potential near the gate electrode is constant.

Afterwards, Suzuki [7] presented Shrivastava's model with accurate boundary conditions. Furthermore, Mohaputra et al. [8] developed a model by taking the presence of source/drain electrodes and high *K*-gate dielectric material into an account. Sicard et al. [9] uses the five capacitance SPICE models for the MOS transistor demonstrated the three built-in metal-oxide-semiconductor field-effect transistor (MOSFET) models. They computed the variation of the capacitance at each iteration for the accurate prediction of the switching delay. Recently, we presented power macromodeling technique [10, 11] by using the capacitive models of [9] to estimate the power dissipation of MOS transistors. In this paper, we further solved their [9] SPICE models for more accurate results. Our macromodel computes the total dynamic power of MOS transistors using the lumped sum of the parasitic capacitances. Our model is look-up-table (LUT) based and achieves relatively good accuracy. In our experiments, we take an account of the parasitic capacitances with their dependence on channel length and the width of the transistors. Our modelling approach can be implemented for several MOS transistors.

The rest of this paper is organized as follows. In Section 2 we give a short background of power

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characteristics. In Section 3 and 4, we discuss about our macromodel construction with the load capacitance and its parameters. Propagation delay is described in Section 5. Section 6 explains the experimental results and in Section 7 we summarize our work.

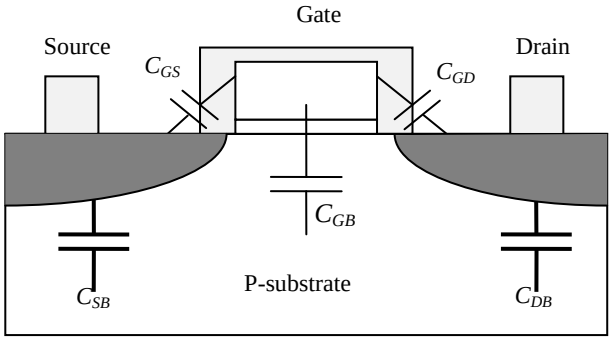


Figure 1. MOS model 3 capacitances

2. Power Macro Model Characterization

In the power estimation of MOS transistors, we must understand where power is consumed. The power dissipation of a MOS transistor is comprised of two types: static and dynamic [12, 13] and can be expressed in (1), (2) and (3) :

$$P_{Total} = P_{Static} + P_{Dynamic} \quad (1)$$

$$P_{Dynamic} = P_{Short-Circuit} + P_{Switch} \quad (2)$$

$$P_{Total} = I_{Leakage} \cdot V_{dd} + I_{Static} \cdot V_{dd} + P_{Short-Circuit} + P_{Switch} \quad (3)$$

Where P_{Total} is total power dissipation. Static power P_{Static} is due to the leakage $I_{Leakage}$ and static I_{Static} currents. The NMOS/PMOS transistors used in a MOS logic circuit commonly have non-zero reverse leakage and sub threshold currents. These currents can contribute to the total power dissipation even when the transistors are not performing any switching action. The magnitude of the leakage current depends mainly on the used technology parameters. The power dissipation of $I_{Leakage}$ is very small and has little effect on the overall dissipation. The I_{Static} occurs in some logic such as pseudo-NMOS logic. Such logic family is usually voided in low power design. Thus, static power dissipation P_{Static} is almost negligible in low power circuit designs.

For the dynamic power dissipation, the first part $P_{Short\text{-}Circuit}$ is caused by direct supply-to-ground paths during the signal transitions. It can be controlled to a small portion of the total power dissipation by appropriate sizing of transistors and reducing the input rise and fall times to all the gates in the circuit. The second part P_{Switch} is due to charging and discharging of parasitic capacitances in the circuit. This is demonstrated by an inverter driving load capacitor C_L shown in figure 2. P_{Switch} can be calculated as:

$$P_{Switch} = V_{DD}^{\ 2} \cdot f \cdot C_L \quad (4)$$

Where V_{DD} is the supply voltage, f is the switch frequency, while C_L is the load capacitance. When the switching occurs in a circuit, C_L is contributed to the total power dissipation. C_L is also called switch capacitance C_{SW}. According to [14], in a "well-designed" circuit, P_{Switch} accounts more than 90% of the total power dissipation. Thus, the total power dissipation for a CMOS circuit can be approximated in (5):

$$P_{Total} \approx P_{Switch} = C_L \cdot V_{DD}^{\ 2} \cdot f \quad (5)$$

Since power is the energy consumed per second, energy E can be stated in eqs. (6) and (7):

$$E = P_{Total} \cdot t \approx P_{Switch} \cdot t = C_L \cdot V_{DD}^{\ 2} \cdot f \cdot t \quad (6)$$

$$E = C_L \cdot V_{DD}^{\ 2} \quad (7)$$

Where *1f /*is the time period of each switch. In a synchronized circuit, t is the clock cycle and f is the clock frequency. Also, C_L is the switch capacitance per cycle. At constant frequency power/energy can be used interchangeably. Further, if we assume the supply voltage V_{DD} is also fixed, reducing the power/energy dissipation is equivalent to reducing the switch capacitance.

Our macromodel is LUT based approach. This model estimates the power dissipation of MOS transistors consists of the function *f(.)* in (8):

$$P = f(V_{DD}, f_{SW}, C_L) \quad (8)$$

Where V_{DD} is the supply voltage, f_{SW} is the switching frequency, while C_L is the load capacitance. The macromodel function *f(.)* in (8) is obtained by a given values of V_{DD}, f_{SW}, C_L, which maps the space to the power dissipation of the MOS transistors. The sub-function $f_{sub}(.)$ in "(9)" can be used to map the space of C_L for *f(.)* in (8):

$$C_L = f_{sub}(C_{GS}, C_{GD}, C_{GB}, C_{DB}, C_{SB}, C_G, C_W) \quad (9)$$

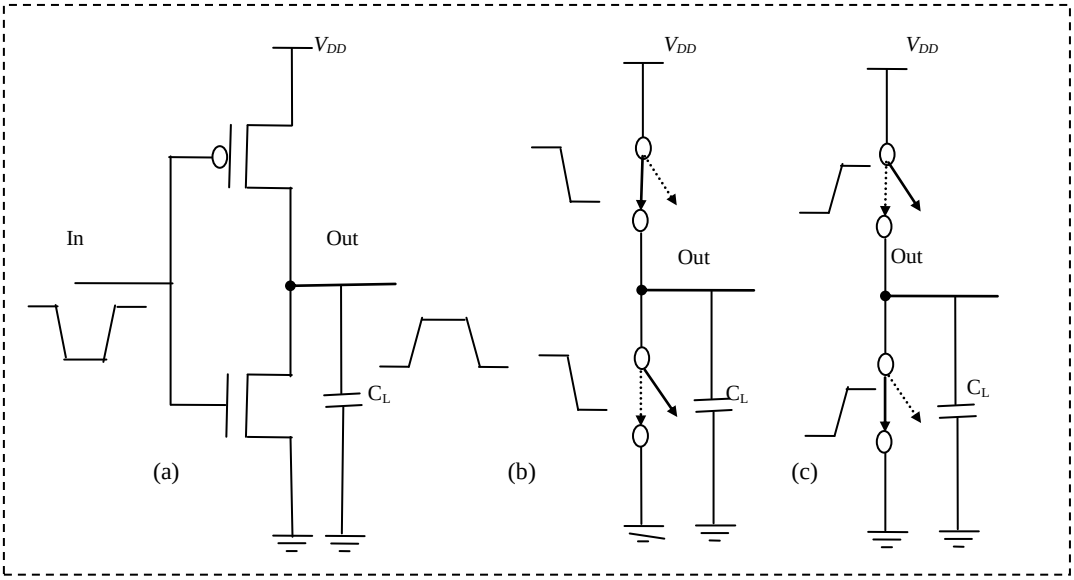


Figure 2. Capacitance switching power: (a) CMOS inverter (b) equivalent circuit for charging the output load capacitor C_L (c) equivalent circuit for discharging the output load C_L.

Where C_{GB}, C_{GS}, C_{GD}, are the *channel* capacitances of gate-to-bulk, gate-to-source and gate-to-drain, while C_{SB}, C_{DB}, are the *junction* capacitances between source-bulk, drain-bulk (as shown in figure 1), C_W is the wire capacitance and C_G is the gate capacitance are derived in (15), (16), (12), (17), (18), (20), (21), respectively. Finally, when the *f(.)* parameters are solely determined, power estimates is a straight-forward and fast function evaluation.

The propagation delay of MOS transistors is dependent on the charging and discharging of C_L. This charging and discharging occurs due to the PMOS/NMOS transistors respectively. Therefore, the dependence of the propagation delay on C_L suggests that getting C_L as small as possible is crucial for the realization of high performance circuits [9].

3. Load Capacitance

Various power estimation techniques [1-4] for MOS transistors using load capacitances have been introduced previously. The load capacitance in (9) consists of parasitic, gate and wire capacitances. The detail is as follows:

3.1 Parasitic Capacitances

In our approach, we consider the primary significant MOS parasitic element is the *gate-to-channel* capacitances (C_{GS}, C_{GD}, C_{GB}) and the secondary element is the *junction* capacitances (C_{DB}, C_{SB}) which both vary in magnitudes. These capacitances are shown in Figure 1, which are depended upon the operational regions and the terminal voltages:

- When the transistor is in *cutoff region* the gate-to-source voltage V_{GS} is less than the threshold voltage V_T i.e. $V_{GS} < V_T$, no channel exists and the total capacitance C_{GC} appears between gate and bulk.
- In the *linear region* with $V_{GS} > V_T$ and a small voltage V_{DS}, is applied between source-drain, an inversion layer is formed which act as a conductor between source-drain. Consequently $C_{GB} = 0$, as the body electrode is shielded from the gate by the channel. In this region the capacitance is distributed between source-drain evenly. In the channel, the velocity of charge carriers is proportional to the electric field E, whereas the carrier mobility is a constant. But this proportionality does not hold for entire range of applied voltage. Due to the gradual increase in V_{DS}, there is a critical value of electric field E_C in which the charge carriers do not follow the linear relationship and the velocity becomes saturates. In other words, there will be no further increase in carrier velocity with the increase in electric field.
- In the *saturation region*, the channel is pinched off. The capacitance between gate-drain is approximately zero, which forms the gate-body capacitance.

Sicard et al. [9] considered five capacitors (C_{GB}, C_{GS}, C_{GD}, C_{SB}, C_{DB}) and implemented the MOS model 3. The variation of the capacitance is computed at each iteration of the analog simulation for the prediction of the switching delay. In our macromodeling approach, we followed their MOS model 3 and further simplified to obtain the new expressions for more accurate results. The procedure is as follows: In the first step, we take MOS model 3 from [9] and implemented the primary parasitic capacitances in (10), (11), (12).

$$C_{GS} = \frac{2}{3}C_i\left[1-\left(\frac{V_{GS}-V_T-V_{DSAT}}{2\ V_{GS}-V_T\ -V_{DSAT}}\right)^2\right] \quad (10)$$

$$C_{GD} = \frac{2}{3}C_i\left[1-\left(\frac{V_{GS}-V_T}{2\ V_{GS}-V_T\ -V_{DSAT}}\right)^2\right] \quad (11)$$

$$C_{GB} = 0 \quad (12)$$

With

$$C_i = W.L\frac{\in_o \in_r}{T_{ox}} \quad (13)$$

Where W is the channel width, L is the channel length, T_{OX} is the oxide thickness, $\in_o$ is the absolute permittivity and $\in_r$ is the relative permittivity.

In our model, we have taken different values of channel width for both PMOS/NMOS transistors. For example we considered L as constant is $0.12\mu m$ for both transistors, and other parameters such as T_{OX} is $3nm$, $\in_o$ is $8.85x10^{-12}F/m$, $\in_r$ is3.9 in case of SiO_2 .

In the second step, we found V_{DSAT} is also a function of V_{GS} and V_T. We further solved V_{DSAT} expression using (14):

$$V_{DSAT} = \frac{V_{GS}-V_T}{1+\frac{V_{GS}-V_T}{E_C L}} \quad (14)$$

Where E_C is the critical electric field at which electron velocity saturation occurs, and it is around $1.5\ V/\mu m$. The saturation velocity V_{SAT} is approximately $10^5 m/s$ and the critical field for holes is $-1.95x10^6\ V/m$. Now by using (14) into (10), (11) we found more simplified expressions of C_{GS}, C_{GD} in (15), (16):

$$C_{GS} = \frac{2}{3}WL\left[1-\left\{\frac{V_{GS}-V_T}{E_C L+2\ V_{GS}-V_T}\right\}^2\right] \quad (15)$$

$$C_{GD} = \frac{2}{3}WL\frac{\varepsilon_\circ \varepsilon_r}{T_{ox}}\left[1-\left\{\frac{E_C L+V_{GS}-V_T}{E_C L+2\ V_{GS}-V_T}\right\}^2\right] \quad (16)$$

In the third step, we have taken secondary parasitic capacitances C_{SB}, C_{DB} from [10] using (17), (18) in our macromodel sub-function $f_{sub}(.)$:

$$C_{DB} = W.L_{drain}\frac{C_J}{\left(1-\frac{V_{BD}}{PB}\right)^{MJ}} \quad (17)$$

$$C_{SB} = W.L_{source}\frac{C_J}{\left(1-\frac{V_{BD}}{PB}\right)^{MJ}} \quad (18)$$

Where W is the channel width, L_{drain} and L_{source} are the lengths of drain and source region of $0.42\mu m$ values. C_J is the junction capacitance around $3x10^{-4}F/m^2$. PB is the built in potential of the junction is around $0.8V$. MJ is called the grading coefficient and equals 0.5 for the abrupt junction and 0.33 for the linear or graded junction.

3.2 Gate Capacitance

Gate capacitance C_G is the total parallel gate capacitance of receiving circuit(s). A typical MOS inverter may drive successive gates and the total C_G. The input capacitances of these gates are also included as a component of C_L. For an inverter, the C_G does not affect the delay because it is not charged or discharged during an output transition. But, it does contribute loading to the previous stage. The two inverters can be switched from the triode region through saturation to cut-off during high-to-low or low-to-high transition. We performed an analysis with non-linear charge storage elements to calculate accurately the total charge supplied to the load inverters. However, the total C_G for the two inverters can be estimated as:

$$C_G = C_{OX}[(W.L)_{p1}+(W.L)_{n1}+(W.L)_{p2}+(W.L)_{n2}] \quad (19)$$

In our design, the L is taken $0.12\mu m$ as the technology parameter, whereas the W of two successive inverters is similar to the first one. Therefore, by using these dimensions (19) can be simplified as:

$$C_G = \frac{2 \in_{0X} L}{T_{OX}} \left[W_p + W_n \right] \quad (20)$$

Where W_p and W_n are channel widths of (PMOS/NMOS) transistors respectively and $\in_{ox}$ is the absolute permittivity.

3.3 Wire Capacitances

Wire capacitance C_W is the total wiring capacitance of the interconnect line (metal or poly). In other words, C_W is a function of its shape, its environment, its distance to the substrate, and the distance to surrounding wires. Due to charging and discharging C_W may dominate the energy budget. Rabaey *et al* [15] developed the C_W model in (21):

$$C_w = C_{pp} + C_{fringe} = \frac{w \varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log\left(t_{di} / H \right)} \quad (21)$$

Where C_{pp} is the parallel plate capacitance, C_{fringe} fringing capacitance, w is the orthogonal field between wire of width and the ground plane, H is the interconnect thickness, t_{di} and ε_{di} represents the thickness of the dielectric layer and its permittivity. From (21), our calculated value for C_W is *0.12fF*.

4. Model Parameters

For any particular model which built for a particular technology range, there must be well defined parameters that hold for every experimental iteration. In our experiments, we have taken the following parameters: Threshold voltage V_{TO} for NMOS/PMOS is *0.4, -0.4V*, carrier mobility U_0 is *0.06, 0.025m²/V.s*, gate oxide thickness T_{OX} is *3nm*, surface potential at strong inversion *PHI* is *0.3V*, bulk threshold parameter *GAMMA* is $0.4V^{0.5}$, saturation field factor *KAPPA* is $0.01V^{-1}$, maximum drift velocity *VMAX* for NMOS/PMOS is *150, 100km/s*, and MOS channel length *L* is $0.12\mu m$ respectively.

In the deep submicron technology, the integrated circuits (IC) with low voltage internal supply and high voltage input/output (I/O) interface are common. Parasitic capacitances in (12), (15), (16), (17) and (18) are implemented at *1.2V*, whereas the I/O devices can be operated at standard voltages (*2.5, 3.3* or *5V*). Another reason for the lower internal voltage operation is the thermal breakdown of oxide layer. The gate oxide thickness is fixed at *3nm* in order to get increased switching performances. Due to the fact that the molecular distance of SiO_2 *is 20A°*, i.e. *10* atoms, the oxide may be destroyed by a voltage higher than a maximum limit V_C called the breakdown voltage. According to [16], the first order estimation is *0.1V/A°* is expressed in (22):

$$V_C = \frac{K}{T_{OX}} \quad (22)$$

Where K is breakdown coefficient and V_C is critical breakdown voltage. Another parameter related to gate oxide thickness is the gate oxide capacitance C_{ox} in (23):

$$C_{OX} = \frac{\in_{OX}}{T_{OX}} \quad (23)$$

From (23), the increase of T_{ox} causes C_{ox} to decrease, therefore reducing drain current I_{DSAT} causes threshold voltage V_T to increase [17].

5. Propagation Delay

The propagation delay or gate delay t_p is the length of time (from input to output) when the gate becomes stable and valid. Propagation delay increases with the operating temperature, marginal supply voltage as well as an increased C_L. The C_L is the largest contributor to the increase of propagation delay. If the output of a logic gate is connected to a long trace or used to drive many other gates (high fan-out) the t_p increases substantially. The overall t_p of the inverter is defined as the average of t_{pHL} and t_{pLH} as given in (24) :

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right) \quad (24)$$

With

$$R_{eq} = \frac{1}{V_{DD}/2} \int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}} \frac{dV}{1 + \lambda V} \quad (25)$$
$$\approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{7}{9} \lambda V_{DD} \right)$$

and

$$I_{DSAT} = K' \frac{W}{L} \left[V_{DD} - V_T \; V_{DSAT} - \frac{V^2_{DSAT}}{2} \right] \quad (26)$$

Where t_{pHL} , t_{pLH} is the delay time from high-to-low and low-to-high propagation, R_{eqn}, R_{eqp} is the equivalent on-resistance of NMOS/PMOS transistors respectively. For the accuracy of our model, we also simplified the R_{eq} in (24) by using (25) and (26) in (27):

$$R_{eq} = \frac{LV_{DD}}{6K'V_{DSAT}}\left(\frac{9-7\lambda V_{DD}}{2V_{DD}-2V_T-V_{DSAT}}\right)\frac{1}{W} \quad (27)$$

It shows that, R_{eq} in (27) is directly linked with the channel width of the device.

6. Experimental Results

In this section, we show the results of our LUT based power macromodeling approach. We have implemented this approach and built the power macromodel to estimate the power consumption of the deep submicrometer conventional MOS transistors. In the first step, we have calculated each transistor's (NMOS/PMOS) primary/secondary parasitic capacitances from (15), (16), (12), (17), (18). For both transistors, the channel length *L* is taken constant of *0.12μm*, whereas the channel width *W* is varied for the specific range using model parameters given in Section 4. For the design of MOS circuits, we do not recommend the same *W* for both (PMOS/NMOS) transistors. As the PMOS switches, half of the current uses the NMOS transistor. The origin of this mismatch can be seen in the general expression of current delivered by both transistors in (28), (29):

$$I_{DS}(NMOS) = \frac{\in_o \in_r \mu_n W_{NMOS}}{T_{OX} L_{NMOS}} \quad (28)$$

$$I_{DS}(PMOS) = \frac{\in_o \in_r \mu_n W_{PMOS}}{T_{OX} L_{PMOS}} \quad (29)$$

We have observed, if W_{NMOS}=$W_{PMOS,}$ and L_{NMOS}=L_{PMOS}, then the current delivered by both transistors will be proportional to electrons and holes mobility respectively i.e. I_{DS} *(NMOS)* α μ_n, and I_{DS} *(PMOS)* α μ_p. The typical mobility values are:

μ_n = 0.068 m²/V.s for electrons

μ_P = 0.025 m²/V.s for holes

Consequently the current delivered by the NMOS is more than twice of the PMOS transistor. We designed MOS transistors with balanced current to avoid significant switching discrepancies. In this case, balanced current and switching performances are required. Several techniques have been introduced previously to counter-balance the intrinsic mobility difference such as to increase the NMOS channel length or to decrease the NMOS channel width but the major drawbacks of these design techniques are the spared silicon area and less consumption of silicon space respectively. The most effective technique is to enlarge the PMOS channel width, as it directly proportional to the current delivered by the PMOS transistor. In our design, we have taken the PMOS channel width twice of NMOS transistor. Therefore, the amount of current is almost doubled and comparable with the NMOS current [9].

The NMOS/PMOS channel widths are taken of specific range between [*0.4μm-1μm*] and [*0.2μm-0.5μm*] respectively. While their corresponding calculated values of the parasitic capacitances are shown in Table 1.

In the second step, our sub-function f_{sub}*(.)* in (9) calculates C_L which includes all parasitic, wire, and gate capacitances as discussed in Section 3. This is a considerable simplification to fit all capacitances in one function. Our simplified f_{sub}*(.)* can be used for large MOS circuits (consist of several transistors) and viewed as one large capacitor that is charged and discharged between the power-supply rails. Therefore, C_L is often specified as power dissipation capacitance and it is used to approximate the dynamic power consumption $P_{dynamic}$. In CMOS circuits, $P_{dynamic}$ dissipates power during the switching activities only. After computing C_L in (9), our macromodel function *f(.)* in (8) estimates power with different voltages and frequencies. For example, at 1-GHz frequency our model estimates the power in table 2.

It is evident from Table 2 that there is a linear relationship between the dynamic power and the load capacitance. From our experimental results, we also found a small change in C_L causes a considerable change in $P_{dynamic}$. This change is more significant in large memory circuits and plays an important role in the VLSI circuit performance. We also observed that a slightly change in channel width and length causes significant change in power consumption e.g. change of W_{NMOS} is *0.05μm* and W_{PMOS} is *0.01μm* causes change of power is *0.504μW*. Power grows linearly with the increase of frequencies as shown in Figure 3.

We compare our estimated power results with the simulated power to evaluate the accuracy of the macromodel function *f(.)* in (8). Reference values are obtained in Multisim simulator. We performed transient analysis for power dissipation

Table 1. Capacitances for NMOS Transistor

Capacitance for NMOS Transistor				
W(µm)	C_{GS}(F)	C_{GD}(F)	C_{SB}(F)	C_{DB}(F)
0.4	2.98E-16	2.51E-16	5.04E-17	4.51E-17
0.5	3.73E-16	3.14E-16	6.30E-17	5.63E-17
0.6	4.47E-16	3.77E-16	7.56E-17	6.76E-17
0.7	5.22E-16	4.39E-16	8.82E-17	7.89E-17
0.8	5.96E-16	5.02E-16	1.01E-16	9.02E-17
0.9	6.71E-16	5.65E-16	1.13E-16	1.01E-16
1	7.45E-16	6.28E-16	1.26E-16	1.13E-16
Capacitances for PMOS Transistor				
0.2	1.47E-16	1.28E-16	2.52E-17	2.91E-17
0.25	1.84E-16	1.60E-16	3.15E-17	3.64E-17
0.3	2.20E-16	1.92E-16	3.78E-17	4.36E-17
0.35	2.57E-16	2.24E-16	4.41E-17	5.09E-17
0.4	2.94E-16	2.56E-16	5.04E-17	5.82E-17
0.45	3.30E-16	2.88E-16	5.67E-17	6.55E-17
0.5	3.67E-16	3.21E-16	6.3E-17	7.27E-17

Table 2. Power Calculations for CMOS Circuit

Ctot (F) (NMOS)	Ctot (F) (PMOS)	Cg (F)	Cl (F)	Power (W)
3.22E-16	6.23E-16	4.25E-16	1.64E-15	2.36E-06
4.02E-16	7.78E-16	5.31E-16	1.99E-15	2.86E-06
4.82E-16	9.34E-16	6.37E-16	2.34E-15	3.37E-06
5.63E-16	1.09E-15	7.43E-16	2.69E-15	3.87E-06
6.43E-16	1.25E-15	8.50E-16	3.04E-15	4.37E-06
7.23E-16	1.40E-15	9.56E-16	3.39E-15	4.88E-06
8.04E-16	1.56E-15	1.06E-15	3.74E-15	5.38E-06

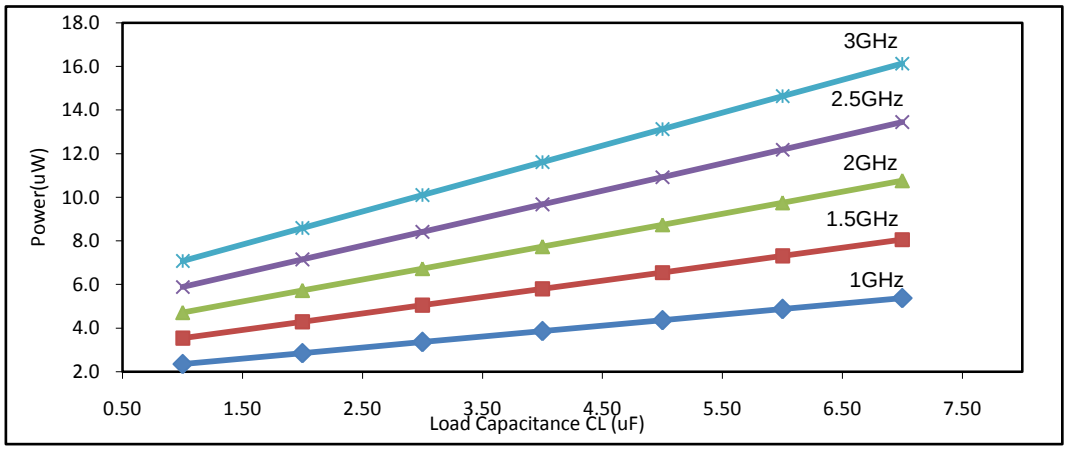


Figure 3. Channel width dependent Power consumption variation.

Table 3. Accuracy of Power Estimation

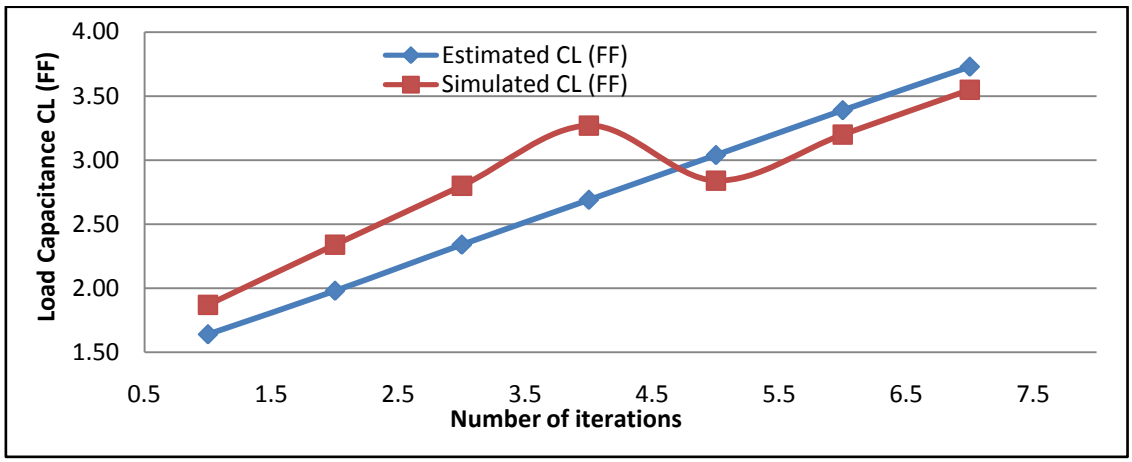
Estimated Power (μW)	Simulated Power (μW)	Error in %
2.36	2.69	12.26
2.86	3.36	14.88
3.36	4.04	16.83
3.87	4.71	17.83
4.37	4.09	6.84
4.88	4.60	6.08
5.38	5.12	5.07

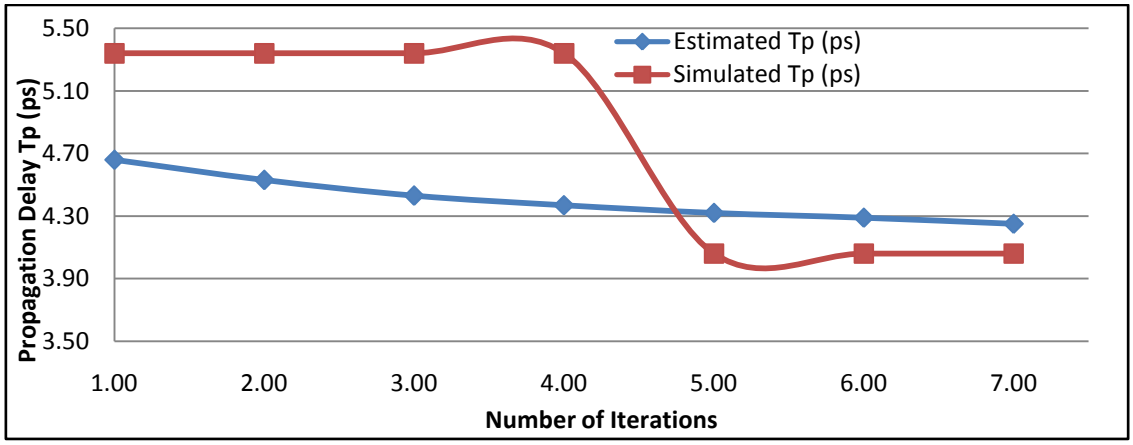
Table 4. Comparison of Estimated and Simulated C_L, t_p

Estimated Cl (ff)	Simulated Cl (ff)	Error in %	Estimated tp (ps)	Simulated tp (ps)	Error in %
1.64	1.87	12.30	4.66	5.34	12.73
1.98	2.34	15.38	4.53	5.34	15.16
2.34	2.80	16.42	4.43	5.34	17.04
2.69	3.27	17.73	4.37	5.34	18.16
3.04	2.84	19.71	4.32	4.06	6.40
3.39	3.20	5.93	4.29	4.06	5.66
3.73	3.55	5.07	4.25	4.06	4.67

of different values of W with the specific range between [*0.4μm-1μm*] and [*0.2μm-0.5μm*] respectively. Our preliminary results are shown in Table 3 with percentage error. It is evident from this table that our macromodel function *f(.)* is accurate with an average error of 12.8%, and maximum error of 21.7%. Table 4 illustrates the comparison of load capacitance and the propagation delay between simulated and estimated values. Figure 4 demonstrates the graphical comparison of estimated and simulated results of load capacitance, propagation delay and power values respectively. Regression analysis is also performed to fit the model's coefficient. We measured the correlation coefficient that is around 91%. In both cases the variation of power with C_L remains same. The sudden change of simulated power in some iterations is due to the increased value of W causes C_L to increase at the cost of decreased average on-resistance. Furthermore, we observed that the power consumption is linearly proportional to the clock frequency and increases gradually with the increase in C_L.

We have presented LUT based new power macromodeling technique for the power estimation of CMOS transistors using *0.12μm* technology. Our model considered all internal parasitic capacitances that includes transistor sizing in order to estimate the dynamic power dissipation. We have discussed a brief description of these parasitic capacitances related to channel and junctions with their precise equations. These equations are simplified and each capacitance is calculated for different values of channel width for both NMOS/PMOS transistors. By using these capacitances the load capacitance is computed and fitted into our macromodel function. Furthermore, simulations are performed for the same channel dimensions and the transient response is used to calculate the power consumption. The estimated and simulated results are compared and the analysis of power consumption with increasing frequency is also done. In our preliminary work, our macromodel showed an average error of 12.8% and a correlation coefficient of around 91%. Currently, we are evaluating our macromodel on more complex circuits and trying to improve its accuracy.





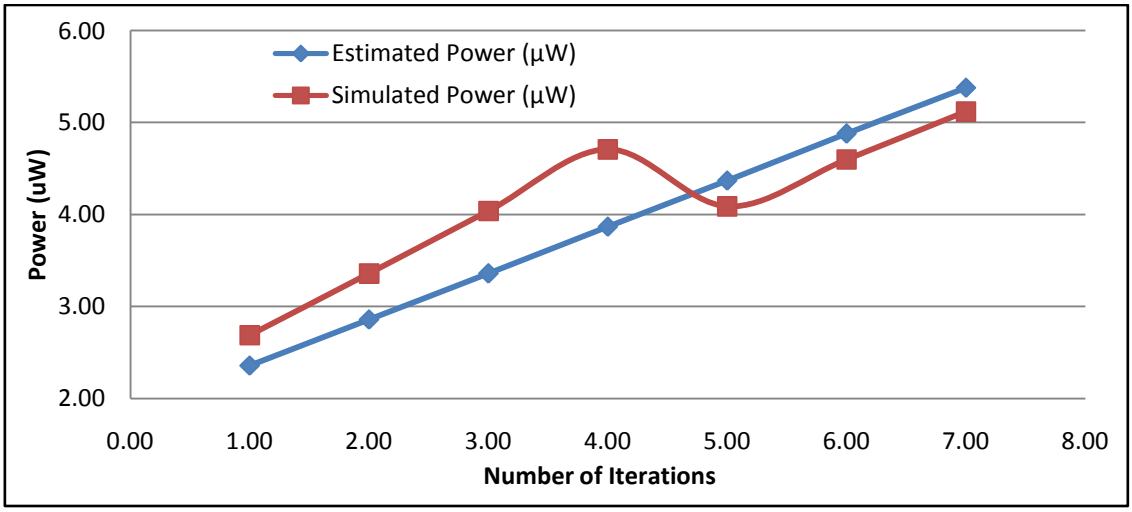


Figure 4. Comparison of estimated and simulated results of load capacitance, propagation delay and power values.

References

[1] G. Consentino and G. Ardita, A Simplified and Approximate Power MOSFET Intrinsic Capacitance Simulation: Theoretical Studies, Measures and Comparisons, Proc. of IEEE Int. Sym. on Industrial Electronics, (2009) pp. 38-43.

[2] S. Ekbote et al., Test Structure Design, Extraction and Impact Study of FEOL Capacitance Parameters in Advanced 45nm Technology, ICMTS (2009) pp. 226-230.

[3] V. D. Kunz, T. Uchino, C. H. Groot, P. Ashburn, D. C. Donaghy, S. Hall, Y. Wang and P. L. F. Hemment, IEEE Transactions on Electron Devices **50** (2003) 1487.

[4] F. Pregaldiny, C. Lallement and D. Mathiot, Solid-State Electron **46** (2002) 2191.

[5] H. Kamchouchi and A. Zaky, IEEE Trans. Electron Devices **ED-30** (1983) 183.

[6] R. Shrivastava and K. Fitzpatrick, IEEE Trans. Electron Devices **ED-29** (1982) 1870.

[7] K. Suzuki, IEEE Trans. Electron Devices **46** (1999) 1895.

[8] N. R. Mohaputra, M. P. Desai, S. G. Narendra and V. R. Rao, IEEE Trans. Electron Devices **50** (2003) 959.

[9] E. Sicard and S. D. Bendhia, Basics of CMOS Cell Design, Mc-Graw-Hill, ISBN 0-07-150906-2 (2007).

[10] Y. A. Durrani and S. Shahbaz, Power Macromodelling for SRAM Cell using 0.12um Technology, Proceedings for 3rd Symposium on Engineering Sciences (March 2010) pp. 195-200.

[11] Y.A. Durrani and B. Arif, Power Macromodelling for DRAM Cell using 0.12um Technology, Proceedings for 3rd Symposium on Engineering Sciences (March 2010) pp. 215-217.

[12] J. M. Rabaey and M. Pedram, Low Power Design Methodologies, Kluwer Academic Publisher, Inc. (1996).

[13] J. Frenkil, Issues and Directions in Low Power Design Tools: An Industry Perspective, Proceeding of International Symposium on Low Power Electronic Design (1997) p. 152.

[14] A. P. Chandrakasan, S. Sheng and R. W. Brodersen, IEEE Journal of Solid-State Circuit 27, No. 4. (1992) 473.

[15] J. M. Rabaey, A. Chandrakasan and B. Nikolic , Digital Integrated Circuit, 2nd Ed., Prentice Hall Publisher (2003).

[16] Albert Z.H. Wang, On Chip ESO Protection for Integrated Circuits, An IC Design Perspective, Kluwer Academic Publishers, ISBN 0-7923-7647-1 (2002).

[17] X. Chen and D. Velencies, I.R.E.E **1**, No. 123 (2006) 513.